Decimation Filter Design

Miljana Sokolovic, Borisav Jovanovic, and Milunka Damnjanovic

Abstract – Decimation filters' architecture for an integrated power-meter is presented in this paper. It is based on parallel processing techniques and inherent pipelining and offers advantages in high speed operation, low power consumption and low complexity for VLSI implementation. The design process consists of several steps, and a full design procedure from the high level coefficients calculation to the synthesis phase performed using SE tools of Cadendce design system is given here. Digital filters are realized using Alcatel CMOS 0.35 technology and its library elements.

I. INTRODUCTION

In digital signal processing systems, digitizing sampled signals at the highest frequencies are preferred due to many advantages of the digital technology. In wide-band applications, signal bandwidth has increased to tens of MHz, so oversampling frequency of A/D converters would be hundreds of MHz or even GHz. In order to isolate the signal of interest from the digitized signals and decimate it to lower sampling rate, high speed decimation digital filters are required [1].

Digital filters described in this paper are part of an integrated power-meter, which is a mixed-signal system that consists of analog CMOS circuits and digital signal processing blocks including these filters. Integrated power-meter DSP chain has two inputs: for the current and for the voltage, and though it requires two signal processing lines. Each input signal is processed within the appropriate sigma-delta modulator. Sampled current signal passes through a third order sigma-delta modulator, while voltage signal passes through the second order modulator. Together with sigma-delta modulators, decimation filters form an A/D converter.

I our case, decimation factors of the filters' chains are 128. This offers a number of possibilities for their structure. The choice is made according to facts that it is better to reduce the sampling frequency as early as possible, then, the more blocks the decimator has, the less their hardware is, and also, that previous steps in the processing chain are second and third order sigma-delta modulators. Requirements for the attenuation in the stopband are 60dB in the voltage filter chain and 80dB in the current filter chain.

A brief overview of the decimation filter's architecture is provided in Section II. In Section III, a VLSI implementation of these architectures is described in more detail. Synthesis and simulation results from the implementation are presented in Section IV. Main filters' properties are also discussed here.

II. DECIMATION LINE ARCHITECTURE

Each decimator consists of 4 blocks, as shown in Figure 1. There are 2 Sinc filters and 2 FIR filters. The first stage has a heavy impact on the total number of digital filter operations. Because the first stage works at the highest data rate, most computational power is concentrated in it. For this reason, a standard FIR filter architecture is not considered adequate for the first stage of a decimator. Instead, an entirely different architecture is implemented [2]. In fact, a non-flat in-band frequency response can be easily allowed for and, hence, equalized in the following stages where the total computational power can be dropped by roughly an order of magnitude. In general, a Sinc filter is chosen as the first and the second stage because it can be conveniently implemented in a very efficient manner.

Furthermore, in the first stages the antialiasing requirements are highly relaxed, which gives the designer a chance to trade frequency distortion for lower power. This is exactly the purpose of a Sinc filter [3]. A limited amount of frequency distortion is introduced into the signal band, confirming the use of a very efficient Sinc architecture. Then, this distortion has to be equalized in the following stages of the decimator, but the cost of this operation is usually almost negligible.

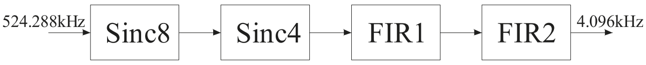

Fig. 1. Architecture of the decimation filters chain

The simplest example of a Sinc filter is the comb filter. An N-tap comb filter is a linear system that calculates the mean value of the last N input samples. Also, a high-order H(z) filter can be split into two lower-order filters. The filters coefficients can be simplified to be simple integers, and according to this, each comb filter has all its coefficients equal to one so addition can be used instead of multiplications. This is especially useful for the first stage of a decimation filter, where the input data rate is the highest. For our example, Sinc stage consists of two Sinc filters with decimation factors 8 and 4 respectively.

Considering signal lines and required values for the attenuation outside the band, two different Sinc stages are used: one for the current channel, and one for the voltage

M. Sokolovic, B. Jovanovic, and M. Damnjanovic are with the Department of Electronics, Faculty of Electronic Engineering, University of Nis, Aleksandra Medvedeva 14, 18000 Nis, Serbia & Montenegro,
E-mail: miljana@venus.elfak.ni.ac.yu

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channel. In the current Sinc stage a fourth order Sinc filters are used, while in a voltage Sinc stage third order Sinc filters are used. This is performed due to the fact that number of sections for each filter block, which is its order, has to be greater at least by one than corresponding sigma-delta modulator on the same line. This rule is employed to FIR filters also.

Considering everything mentioned, architectures for Sinc filters for both channels are obtained and they are shown in Figure 2. For example, cascading three accumulators followed by three cascaded differentiators realize one voltage channel Sinc filter. It can be seen that a switch working at lower frequency is placed between these two cascades. The differentiators' part clocking frequency is 8 times less comparing to the input sampling frequency. In this way, decimation is performed. Lengths of input and output words are obtained according to required memory size and the error magnitude.

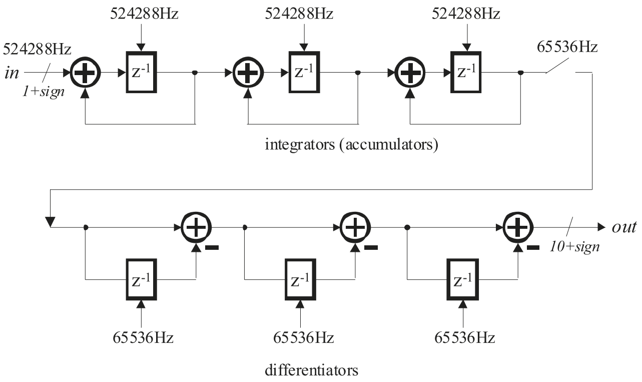


Fig. 2. Architecture of the first voltage Sinc stage

The second stage of the decimator has to equalize the frequency distortion introduced by the Sinc stage. Moreover, since this is a decimation stage also, an antialiasing frequency response is required. This stage consists of two FIR filters. The decimation factor for each FIR filter is 2, in each line. The first FIR filter in a chain corrects the distortion implied by the first two Sinc blocks. This is also a low-pass filter and though it has to provide a noise shaping outside the filter bandwidth. The last FIR filter is used as an element with a very high selectivity.

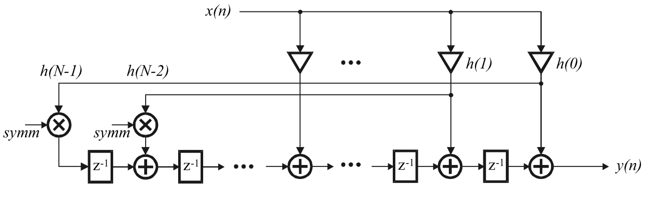


Fig. 3. Internal structure of the FIR filter

FIR filters' design is based on a CSD (Canonical Signed Digit) representation, and they have a hardwired implementation of their coefficients. Their internal structure is shown in Figure 3. This kind of realization enables savings in area and power consumption, while accomplishing high working frequencies [3]. For the filter coefficients design, there are number of advantages provided by CSD code over the ordinary binary representation. First, since there are no adjacent nonzero digits in CSD code, one may expect less nonzero digits in CSD code than in the binary equivalent, which simplifies filter implementation. For the similar reason, CSD code is expected to be less sensitive to truncations which can further help in reducing add-shift operations within the multipliers while preserving initial filter properties. Therefore, the following filter design strategy is adopted for this particular project:

a) Determine ideal filter coefficients for the target amplitude response. This is accomplished via least mean square (LMS) based optimization procedure for linear phase FIR filters design [3].

b) Convert ideal (infinite precision) coefficients to a set of integers that is finite precision coefficients.

c) For each integer coefficient determine its CSD representation using the algorithm given in [3].

d) Truncate CSD representation by keeping only most significant nonzero digits.

Number of filter taps N, and coefficients are varied until the desired filter response is achieved. In order to have more efficient hardware implementation, they all are optimized to be as low as possible.

As can be seen from the Figure 3, the structure is symmetrical. By using the CSD filter coefficients representation, multiplying operations are replaced with shifting and adding operations.

III. VLSI Implementation

All described filters use just several different digital building blocks. They are all listed in Figure 4. The corresponding time domain equation is also given for each block. Due to this, a much easier VLSI implementation can be expected [4].

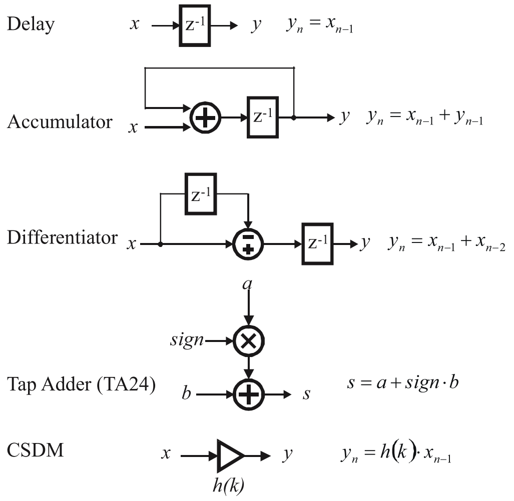


Fig. 4. Filters' building blocks

Each one of these blocks was described in VHDL, and in that way, some kind of filters' library elements were created. It was very easy to instantiate each one of them and to create bigger filter blocks. In order to reuse the same blocks, lengths of input and output digital words were described as *generics*. Each filter block contains additional control logic, which is not shown here. It should be noticed that every filter block has two different clock input signals: one for the input sampled word and one for the output, decimated digital word.

Considering Sinc filters implementation shown in Figure 2, VHDL block diagram in Figure 5 can be generated. It is a block diagram of the general third order Sinc filter with a corresponding decimation factor which is equal to *clkin/clkout*. In this case, a decimation factors for the voltage lines are 8 and 4 respectively. For a fourth order Sinc filter, a line would consist of four accumulators and four differentiators. The amplification of the third order Sinc8 filter is $8^3=2^9$, so the length of the output digital word is increased by 9. A similar calculation stands for the other three Sinc filters.

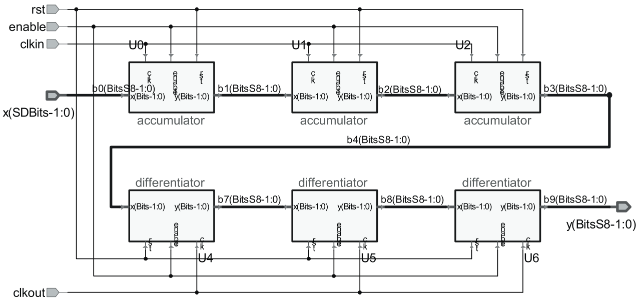


Fig. 5. VHDL implementation of the Sinc filter

As mentioned, symmetrical FIR filters can be effectively constructed using the architecture of Figure 3 with CSD multipliers and tap adders. The implementation of the first voltage channel FIR filter will be discussed next in more details. Coefficients obtained by a specific C program are listed in Table I. All odd coefficients are equal to zero, so additional area savings and distortion reductions can be performed in this way.

TABLE I
COEFFICIENTS FOR THE FIRST VOLTAGE CHANNEL FIR FILTER

Coefficient	Values	CSD representation
h(0) = h(10)	0.0117188	1 x (+1/2^6 -1/2^8)
h(1) = h(9)	0	0
h(2) = h(8)	-0.0625	1 x (-1/2^4)
h(3) = h(7)	0	0
h(4) = h(6)	0.300781	1 x (+1/2^2 +1/2^4 -1/2^6 +1/2^8)
h(5)	0.5	1 x (+1/2^1)

Obtained FIR filter implementation is shown in Figure 6. It consists of six tap adders. CSDM block is used for hardwired coefficients calculation. Dividing operations are replaced with a simple shifting, which is here denoted using "<<" symbols. Blocks denoted with "z^{-1}" are realized as delay lines implemented using flip-flops. Clock signals are not shown in this Figure.

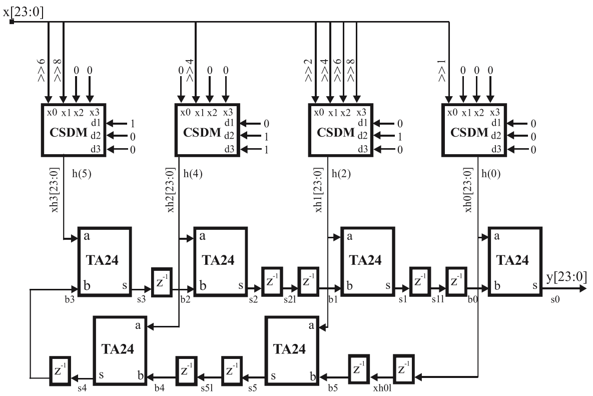


Fig. 6. Implementation of the FIR filter

Other FIR filter blocks have different number of tap adders. There are: second voltage channel FIR filter, 15 tap adders, first current channel FIR filter, 7 tap adders and second current channel FIR filter, 17 tap adders.

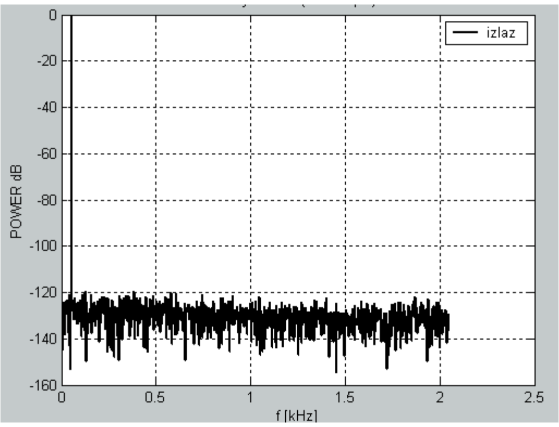
IV. SYNTHESIS AND SIMULATION RESULTS

Digital filters described in VHDL were first verified in VHDL simulator Active HDL. A test bench was written for each digital filter, with input stimuli and clock signal defined. Simulation results (digital samples on filter's outputs) were loaded in Matlab program package in order to perform FFT over them. Derived spectra met all requirements.

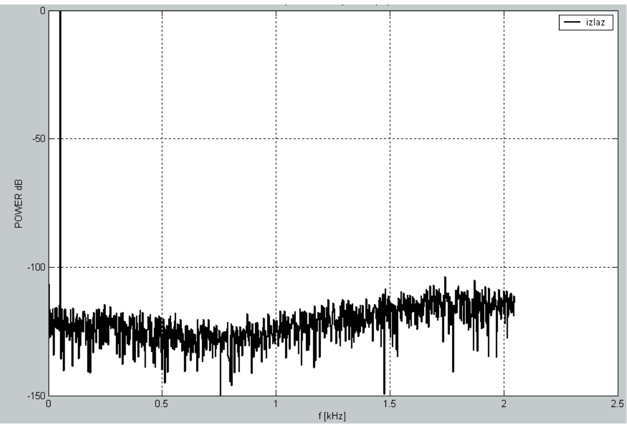
TABLE II
AREA OF FILTER BLOCKS

Filter	Area in NAND gates units	Area in square µm
FIRV	10006.08	754.5µm x 1084.5µm
FIRC	11704.42	898.5µm x 1048.5µm
SINKV	2296.29	760.5µm x 280.5µm
SINKC	3265.12	901.5µm x 322.5µm

Then, VHDL filters descriptions were loaded into program for logical synthesis, Build Gates, which is a part of Cadence design system [5]. Build Gates generates netlist consisting of Alcatel CMOS035 digital library cells. In order to perform synthesis process correctly, it is necessary to specify clock and reset trees as untouchable during the synthesis process. Because of several different clocks signals it is also necessary to specify timing relations between them precisely. Clock and reset tree generation were performed during floorplanning, placement and routing process using program called Silicon Ensemble. After completed synthesis processes, area of filters could be estimated expressed in logical NAND gates units. Filters areas are given in Table II. FIRV denotes a chip block that consists of both FIR filters for the voltage channel, FIRC denotes a chip block that consists of both FIR filters for the current channel, SINKV denotes a chip block that consists of both voltage Sinc filters, and finally SINKC denotes a chip block that consists of both current Sinc filters.



a) current channel



b) voltage channel

Fig. 7. Obtained FFT results

During synthesis process, standard cells' netlist was extracted, and in a form of Verilog file loaded back to VHDL simulator. The simulation was now performed using Cadence' NCsim tool, which is a tool for logical verification, using the same test bench as before synthesis process. Results of this simulation are digital samples from the filters' outputs. They are again loaded back to Matlab and processed with FFT functions. Obtained frequency spectra were unchanged, and they are shown in Figure 7. In this way, a design verification process was completed successfully, since the requirements are met.

Here, it can be seen from Figure 7 that the attenuation in the stopband for the total current decimation stage is greater then 120dB, while the attenuation for the voltage stage is greater then 110dB.

Using Cadence' program Silicon Ensemble, floorplanning, placement and routing were performed, as well as clock and reset trees generation. At the end, Verilog file is extracted and brought back to NCsim simulator where final check of the total digital part of the chip was performed. Filters blocks' areas obtained in this way are also listed in the Table II.

V. CONCLUSION

Digital decimation filters have proven their worth in a variety of applications. They can provide advantages in terms of speed, power, chip area and efficiency. A strategy for the efficient decimation filter design has been presented. At the highest design level, Matlab program tools have been used for filters' coefficients calculation. Then a VHDL description is written for each filter chain block. The synthesis tool, BG, creates netlist for those descriptions. During this phase, AMI (Alcatel Microelectronics) Semiconductors CMOS035 standard digital library cells have been used. And finally, SE, Cadence tool for floorplanning, placement and routing is used to get final design for production. Post layout simulations proved the consistence of behavioral, gate and transistor level design. At the moment, it is expected to get a prototype of the chip, and after that some measurements can be performed.

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